

High-Level Synthesis of a Generic Cordic Accelerator

Introduction

The Cordic algorithm, which enables the hardware-efficient calculation trigonometric functions, is one of the work horses of digital integrated circuits. Thereby, the optimal hardware architecture highly depends on silicon throughput and area requirements. With this regard, a High-Level-Synthesis approach, for which the integrated circuit is modelled in a high programming language such as SystemC or C, is promising as it enables an easy adaption towards different requirement sets.

void cic:CicThread(){
HLS_DEFINE_PROTOCOL("reset");
din_reset();
wait()
output_tint_reg[4] = {0, 0, 0, 0};
cutput_tint_reg[4] = {0, 0, 0, 0};
cutput_tint_reg[4] = {0, 0, 0, 0};
cutput_tint_reg[4] = {0, 0, 0, 0};
cutput_tint_reg[6] = {0, 0, 0, 0};
cutput_tint_reg[6] = {0, 0, 0, 0};
cutput_tint_reg[6] = {0, 0, 0, 0};
int_reg[6] = int_reg[6] + int_reg[1-1];
int_reg[6] = int_reg[6] + int_reg[6] + int_reg[6];
int_reg[6] = int_reg[6] + int_re

Short Project Description

The goal of this project is to develop a generic Cordic description in C language which can be synthesized to an integrated circuit. The benefit of the approach is proven by synthesizing a Cordic hardware accelerators for different throughput requirements and compare implementation costs to state-of-the-art Cordic implementations.

Prerequisites

- Interest in signal processing and VLSI design
- Basic knowledge in SystemC or C is helpful

What you will learn

After the project you will be able to design digital integrated circuits using a High-Level-Synthesis design flow. In addition, you get familiar with one of the most powerful digital algorithms used in many modern communication systems.

Contact

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